Fundamentals
of Signal Integrity
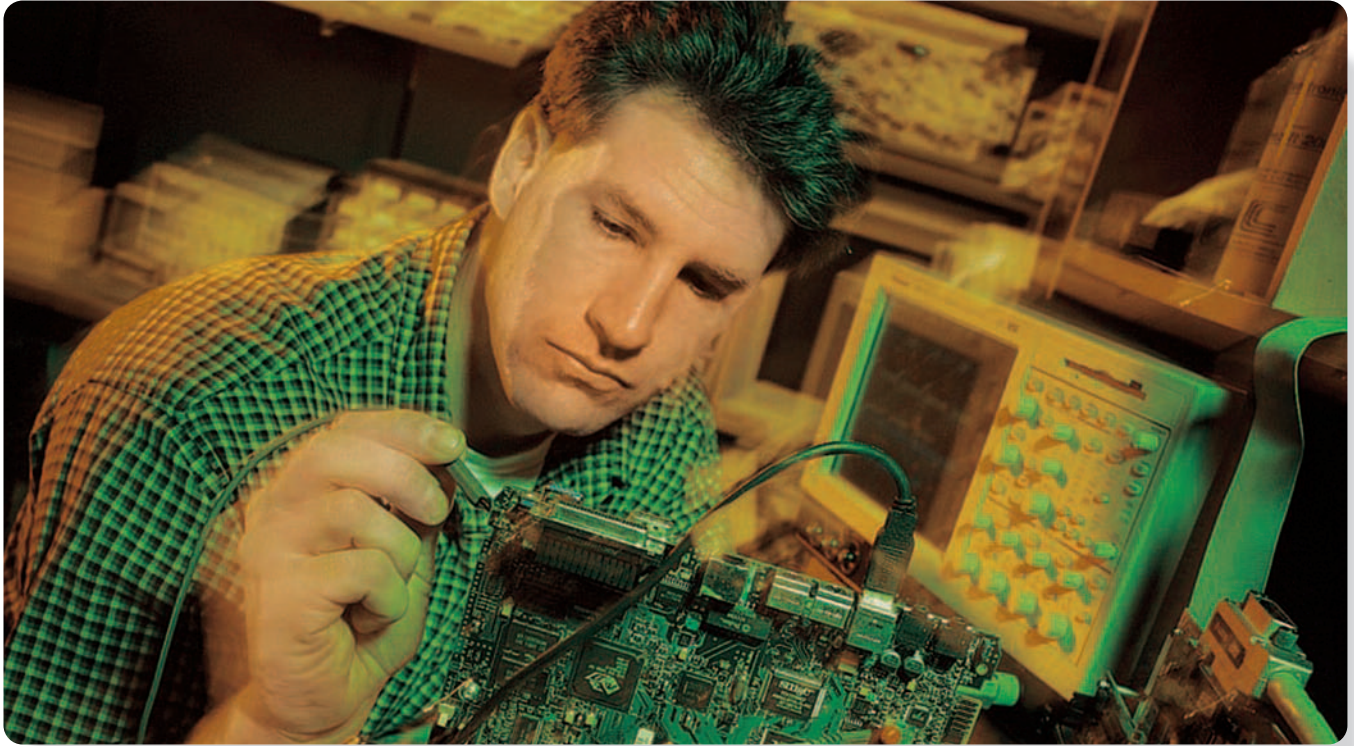
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What is "Signal Integrity?"

In its traditional definition, the term "integrity" means "complete and unimpaired." Therefore, a digital signal with good integrity would have clean, fast transitions; stable, valid logic levels; accurate placement in time; and it would be free of transients. For reasons that will be explained here, it is getting more difficult to produce and maintain complete, unimpaired signals in digital systems. Digital signal integrity has become a pressing concern for system developers.

The purpose of this primer is to provide some insight into the causes, characteristics, effects, and solutions for signal integrity-related problems in digital systems.

Digital Technology and the Information Age

It has been two decades since the personal computer emerged in its current form, and almost 15 years since cellular telephony became a consumer phenomenon. Over that span of time, one trend has been constant: the demand for more features and services, and the bandwidth to deliver them. First-generation PC users who were once excited about the power of a simple spreadsheet now demand graphics, audio, and video. Mobile phone subscribers, once content to simply converse without wires, now expect text messaging, stock quotes, internet browsing, and more.

Businesses, governments, and individuals around the world have come to depend on all this new content and its rapid, reliable delivery. The term "Information Age" was coined to describe today's interwoven, interdependent, data-based culture.

The demand for information has been met with a steady stream of technology breakthroughs in the fields of semiconductors, PC bus architectures, network infrastructures, and digital wireless communications. In PCs (and even more so in the special class of PCs known as servers), processor speeds have escalated into the multi-GHz range; memory throughput and internal bus speeds have risen commensurately.

These dramatically increased rates support computer applications such as 3D games and computer-aided design programs. The textured, shaded 3D images you see onscreen require a huge amount of bandwidth at the circuit-board level, where the CPU, the graphics subsystem, and the memory must move data constantly as the image moves.

Computers are just one facet of the bandwidth-hungry information age. Digital communication equipment designers (particularly those developing the electrical and optical infrastructure elements for both mobile and fixed networks) are exploring 40 Gb/s data rates. And digital video product development teams are designing a new generation of transmission equipment for high-definition, interactive video.

Numerous technologies underpin these data rate advancements. Serial buses are emerging to break the speed barriers inherent in older parallel bus architectures. Components such as Rambus memory devices use a tightly controlled 28-ohm impedance environment (rather than the more common 50 ohms) to ensure signal integrity at maximum clock rates. And smaller, denser circuit boards using ball grid array ICs and buried vias have become common as developers look for ways to maximize density and minimize path lengths.

Designing with Signal Integrity Concepts

Rising Bandwidth Makes Digital Design "Details" More Important

The digital bandwidth race requires innovative thinking. Increasing a system's operating rate is not a matter of simply designing a faster clock. As frequency increases, the traces on a circuit board become more than simple conductors. At lower frequencies (such as the clock rate of an older digital system) the trace exhibits mostly resistive characteristics. As frequencies increase, the trace begins to act like a capacitor. At the highest frequencies, the trace's inductance plays a larger role. All of these characteristics can adversely affect signal integrity.

At clock frequencies in the hundreds of megahertz and above, every design detail is important:

► Clock distribution
► Signal path design
► Stubs
► Noise margin
► Impedances and loading
► Transmission line effects
► Signal path return currents
► Termination
► Decoupling
► Power distribution

All of these considerations impact the integrity of the digital signals that must carry clocks and data throughout a system. An ideal digital pulse is cohesive in time and amplitude; free from aberrations and jitter; and has fast, clean transitions. As system speeds increase, it becomes ever more difficult to maintain ideal signal characteristics. That is why signal integrity is a critical issue. *A pulse rise time may be adequate in a system clocked at 50 MHz, but will not suffice at 500 MHz clock rates and above.* Signal integrity is an issue of growing concern as gigabit data rates become common in digital systems.

Digital Timing Issues Can Cause Signal Integrity Problems

An engineer working with an evolving digital system design is likely to encounter signal integrity problems in their digital form. That is, the binary signals on the bus or device outputs produce incorrect values. The errors may appear in the waveform (timing measurement) view on a logic analyzer; or they may show up at the state or even the protocol level. Remember, one bad bit can dramatically affect the outcome of an instruction or transaction.

Digital signal aberrations stem from many root causes. Timing-related issues are especially common:

► Bus contention occurs when two driver devices try to use the same bus line at the same time. Aberrations will inevitably result. Normally, one of the drivers should go to a high impedance state and stay "out of the way" while the other sends data. If the high impedance device doesn't change in time, the two drivers contend for the bus. Neither driver prevails, forcing the bus to an indeterminate amplitude that may fail to reach the threshold voltage, creating, for example, a "0" logic level where there should be a "1."

► Setup and hold violations can occur in digital systems. A clocked device such as a D flip flop requires the data to be stable at its input for a specified time before the clock arrives. This is known as *setup* time. Similarly, the input data must remain valid for a specified time after the leading edge of the clock. This is known as *hold* time.

Violating setup and/or hold requirements can cause unpredictable glitches on the output, or no output transition at all. Setup and hold time requirements are decreasing as device speeds increase, making the timing relationships harder to troubleshoot.

▶ Metastability is an indeterminate or unstable data state that results from a timing violation such as a setup and hold problem. The resulting output signal may be a glitch that causes problems.

▶ Undefined conditions can occur when the switching states on multiple inputs of a logic device are not correctly aligned in time. This may be caused by variations or errors in the delay on these input signals.

Digital acquisition instruments—logic analyzers in particular—have powerful tools to help users trigger, store, and view digital signals in many formats. Probes attached to the system under test feed data to multiple channels of the logic analyzer. Today's advanced logic analyzers can capture data from thousands of test points at once.

The most basic display mode is the timing display that shows streams of digital pulses and their placement in time relative to one another, as seen in **Figure 1**. The state display (Figure 1) looks at data qualified by a clock signal generated within the unit under test, allowing a designer to evaluate the state of the digital circuit. These results can be further interpreted with the help of disassemblers and processor support packages, which allow the logic analyzer to correlate the real-time software trace (correlated to source code) with the low-level hardware activity. In most instruments this is limited to the digital domain.
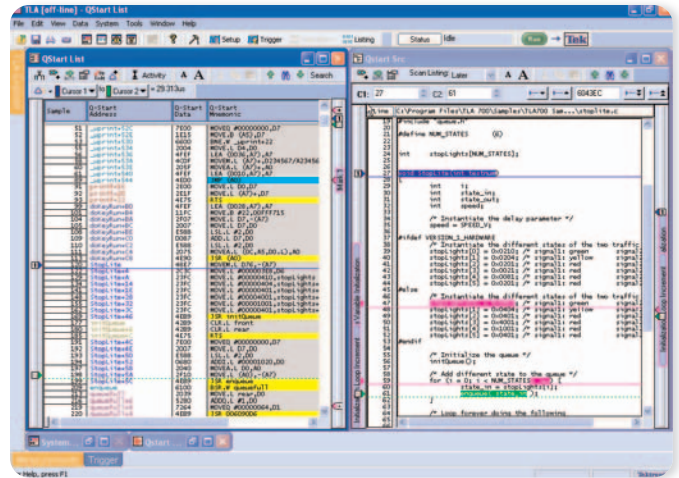

▶ Figure 1. *Logic analyzer display showing timing waveforms and real-time software trace correlated to source code.*

With this type of conventional logic analyzer acquisition, amplitude errors and glitches can appear to be valid logic levels even though they contain incorrect data. You may see an error value in the hexadecimal code, for example, but you cannot see why it is occurring. If you have no means to probe further into the signal's behavior, it can be very difficult to find the cause of the logic error.

Fundamentals of Signal Integrity

▶ Primer
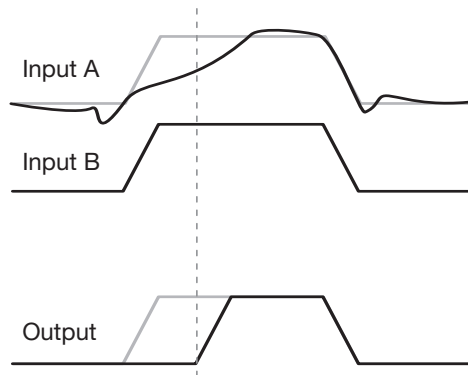
▶ **Figure 2.** *The black trace on Input A is an analog view of the actual signal. The black waveform's slow rise time crosses the threshold late, resulting in a narrowed output pulse. The signal integrity on Input A is very poor.*
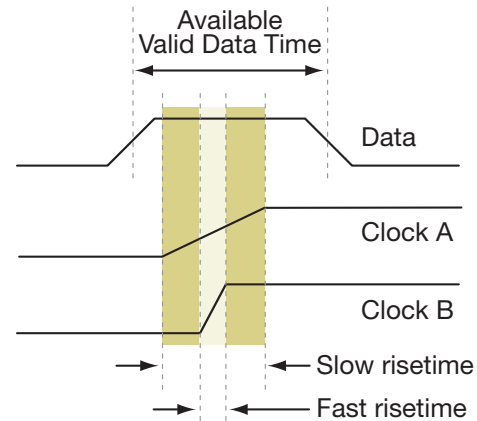
▶ **Figure 3.** *If Clock A is used to clock in the Data, its slow rise time uses up too much data time. The faster Clock B edge leaves more time to deliver the data value. (Not shown to scale.)*

Tracking Down Analog Aberrations

Many digital problems are much easier to pinpoint if you *can* probe deeply into the signal's behavior and see the analog representation of the flawed digital signal. Although the problem may appear as a misplaced digital pulse, the cause of the problem signal could be related to its analog characteristics. Analog characteristics can become digital faults when low-amplitude signals turn into incorrect logic states, or when slow rise times cause pulses to shift in time. Seeing a digital pulse stream with a simultaneous analog view of the same pulses is the first step in tracking down problems like these.

In any discussion of signal integrity, signal transitions deserve special attention. The timing diagram in **Figure 2** explains why. Assume the two inputs are feeding an ordinary AND gate. The gray trace for Input A shows the pulse as it "should be." The distorted black trace superimposed on it is an analog view of the actual signal. Due to its slow rise time, the actual signal does not cross the threshold value until much later than it should. As a result the output pulse is narrower than it should be (the correct pulse width is shown in gray). This problem can cause errors in subsequent logic steps. The integrity of the signal on Input A is very poor, with serious consequences for digital elements elsewhere in the system.

Suppose the output went on to become part of a memory address. The short pulse might cause the memory to see a "0" where there should be a "1," and therefore select an entirely different memory location than that which is expected. The content of that location will of course be completely inappropriate for the transaction at hand. The end result of the transaction will be invalid.

Slow signal transition edges can lead to intermittent system faults even if they are not causing repeatable errors. Timing budgets in the fastest systems allow very little time for the signal's rise and fall transitions. Setup and hold times have dramatically decreased in recent years. Rambus and DDR (double data rate) memories, for example, now specify setup and hold times in the low hundreds of picoseconds.

Slow edges can leave too little margin in the timing budget for the data to be valid and stable, as implied in **Figure 3**. The relationships in Figure 3 are exaggerated to emphasize the concept. A slow transition time on the clock can consume valid data time on the data signal.

These two examples show some of the potential effects of edge problems in a digital system.

Circuit Layout, Transition Times, and Signal Integrity

As we have seen, distorted rise and fall times can be directly responsible for digital faults. Today's fast digital technologies require signals with fast, clean edges.

It is important to remember that many digital systems designed with slower clock rates may still have very fast edges. Semiconductor device technology advances have brought faster edge performance to virtually every logic family. These edges carry high-frequency components, irrespective of the clock rate. Fast edges bring many benefits, but can also add complications to the designer's job.

Present-day bus architectures have rise and fall times in the range of hundreds of picoseconds. Some examples are shown in **Table 1**.

Transition times in this range require the designer to take extra care in making component, termination, and layout choices. Circuit board traces just six inches long act like transmission lines when driven with signals exhibiting transition times below two nanoseconds, irrespective of the clock cycle time.

Digital Device	Transition Time (Rise and Fall Time)
DDR RAM	<250 ps
FireWire IEEE 1394b	80 to 300 ps
InfiniBand	≈100 ps
USB 2.0	>500 ps

▶ **Table 1.** *An overview of digital transition times.*

Today's device technologies have surpassed this transition speed by an order of magnitude, which means that transition speed is a factor to be considered in every digital design.

When edges transition at high speeds, new signal paths are created. These intangible connections do not show up on the schematics, but nevertheless provide a means for signals to influence one another in unpredictable ways. For example, ground planes and power planes become part of the transmission line systems that are formed by the circuit board signal runs, and in turn interact with each other. These interactions have names: crosstalk and ground bounce.

Effects like these are classic analog phenomena. They are at the heart of many failures that plague new digital system designs. The integrity of digital signals relies on their behavior in the analog domain.

Signal Integrity: A Term With Many Meanings

For the purposes of this discussion, a "signal integrity" problem is defined as any phenomenon that can compromise a signal's ability to convey binary information. In real, operating digital devices, these "binary" signals have analog attributes that result from complex interactions of many circuit elements, ranging from the driver outputs to signal path terminations.

Specific problems include:
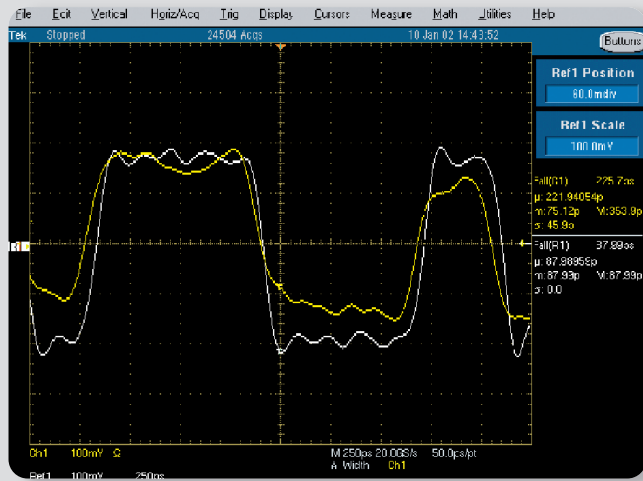
▶ **Amplitude problems**

Amplitude problems include ringing (oscillation), "droop" (decreased amplitude at the beginning of a pulse), and "runt" pulses (those which simply do not reach full amplitude).
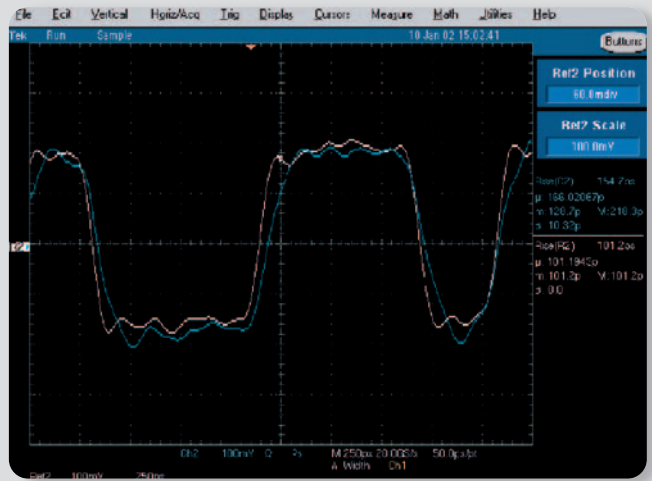
▶ **Edge aberrations**

Edge aberrations can result from board layout problems as described earlier, or from improper termination, or even quality problems in the semiconductor devices. Aberrations include preshoot, rounding, over-shoot, ringing, slow rise time, and more.
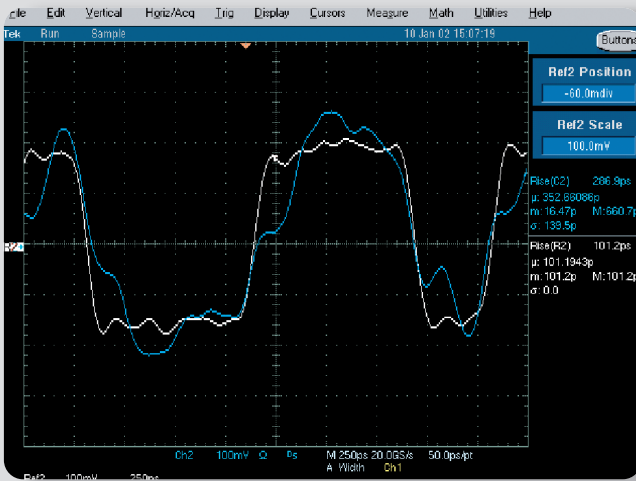
▶ **Reflections**

Reflections can be caused by termination and board layout problems. The outgoing signal can bounce back toward its source and interfere with subsequent pulses.
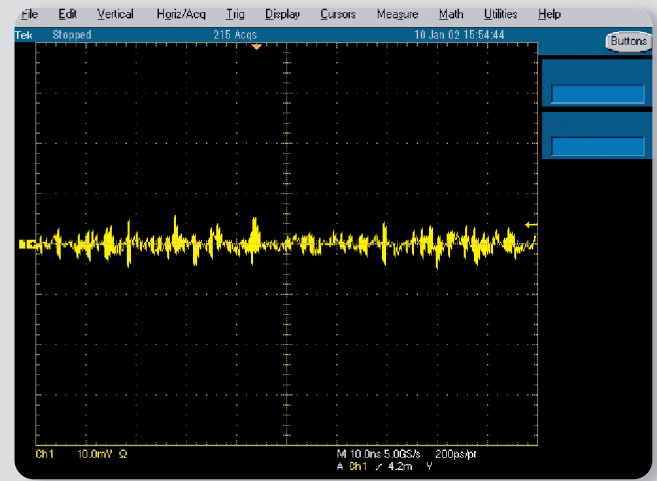

▶ **Ground bounce**

Ground bounce, caused by excessive current draw (and/or resistance in the power supply and ground return paths), can cause a circuit's ground reference level to shift when current demands are high.
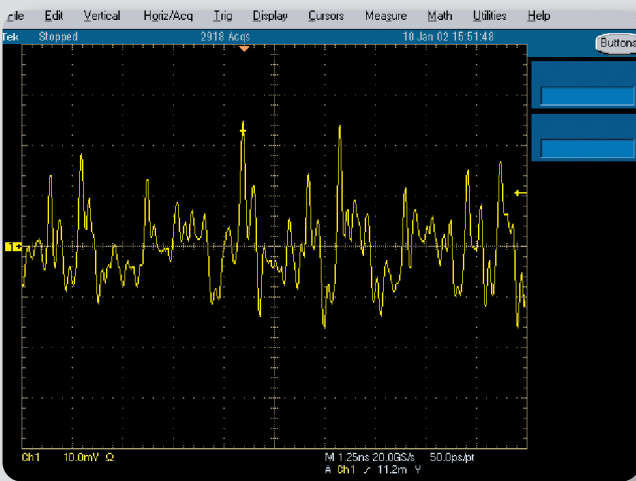
▶ **Crosstalk**

Crosstalk can occur when long traces, running next to each other, can couple their signals one to another through mutual capacitance and inductance. In addition, the higher current embodied in fast edges increases the amount of radiated magnetic energy, and with it, crosstalk.
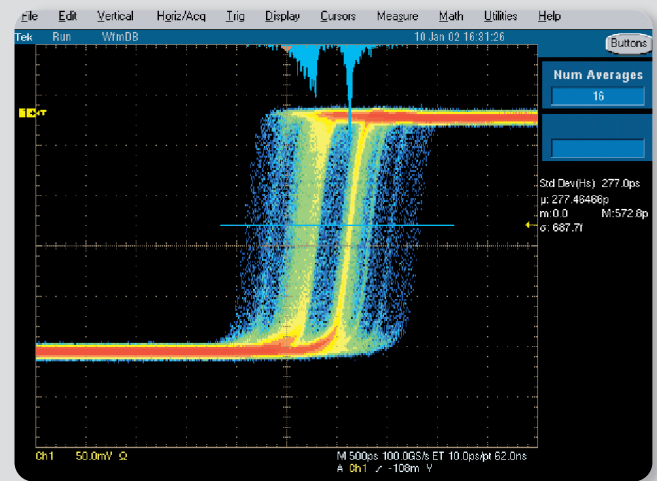
▶ **Jitter**

Jitter arises when digital signals contain tiny edge placement variations from cycle to cycle. This can affect timing accuracy and synchronization throughout a digital system.

Signal Integrity Validation Requirements

Direct signal observations and measurements are the only way to discover the causes of signal integrity-related problems. As always, choosing the right tool will simplify your job. For the most part, signal integrity measurements are carried out by the same familiar instruments found in almost any electronic engineering lab. These instruments include the logic analyzer and the oscilloscope. Probes and application software round out the basic toolkit. In addition, signal sources can be used to provide distorted signals for stress testing and evaluation of new devices and systems.

What are the key questions to ask when assembling a signal integrity measurement setup? The most important considerations include:

▶ Probing—can the measurement instrument transmit signals accurately from the device under test to the acquisition system input? Are the probes reliable and easy to use?

▶ Bandwidth and step response—can the measurement instrument reliably distinguish signal activity (both digital and analog) all the way down to the picosecond range? Possibly the most important measurement characteristics for signal integrity work are oscilloscope bandwidth and step response. These characteristics ensure adequate capture of the signal aberrations that define signal integrity.

▶ Timing resolution—can the measurement instrument properly capture transition times in every data cycle, even at the highest clock rates? The logic analyzer's timing resolution is the key to initially detecting the misplaced pulses and edges that can imply signal integrity problems.

▶ Record length—how many acquisition samples can the measurement instrument store at high sample rates?

▶ Triggering—does the measurement tool have a versatile selection of triggers and more importantly, does it have triggers that can pinpoint signal integrity-related problems?

▶ Display and analysis—can the measurement tool display results such that they are easy to read and interpret?

▶ Integration—does the measurement tool integrate with other instruments to form a balanced digital and analog measurement solution that provides complete system visibility at the digital, analog, and protocol levels?

Logic Analyzer Feature	Recommended Capability for SI Analysis
Oscilloscope integration	Time-aligned oscilloscope traces on logic analyzer screen, multi-channel eye diagrams
Probing	Simultaneous timing, state, and analog acquisition through the same logic analyzer probe
Timing measurement resolution	125 ps (at 8 GHz clock rate)
State acquisition rate	Up to 800 MHz
Acquisition record length	Up to 256 M
Triggering	Edge, Glitch, Logic, Setup/Hold, etc.
Analysis	Processor support packages and disassemblers
Display	Multiple displays

► **Table 2.** *Signal integrity analysis calls for some of the highest available logic analyzer performance.*

Logic Analyzers Discover Digital Faults

As mentioned earlier, the logic analyzer is the first line of defense for digital troubleshooting, especially for complex systems having numerous buses, inputs and outputs. This instrument has the high channel count, deep memory, and advanced triggering to acquire digital information from many test points, and then display the information coherently.

Because it is a truly digital instrument, the logic analyzer detects threshold crossings on the signals it is monitoring, then displays the logic signals as seen by logic ICs. The resulting timing waveforms are clear and understandable, and can easily be compared with expected data to confirm that things are working correctly. These timing waveforms are usually the starting point in the search for signal problems that compromise signal integrity.

Not every logic analyzer qualifies for signal integrity analysis at today's extremely high (and increasing!) digital data rates. **Table 2** provides some specification guidelines that should be considered when choosing a logic analyzer for advanced signal integrity troubleshooting.

With all the emphasis on sample rates and memory capacities, it is easy to overlook the triggering features in a logic analyzer. Yet triggers are often the quickest way to find a problem. After all, if a logic analyzer triggers on an error, it is proof that an error has occurred. Most current logic analyzers include triggers that detect certain events that compromise signal integrity—events such as glitches and setup and hold time violations. These trigger conditions can be applied across hundreds of channels at once—a unique strength of logic analyzers.

Logic Analyzer Probing Solutions

A logic analyzer's probing scheme plays a critical role in high-speed digital acquisition. The probe *must* deliver the signal to the logic analyzer with the highest possible fidelity. Most logic analyzers have mastered this fundamental requirement, but some take the concept even further.

Some logic analyzers require separate probing connections for timing and state acquisitions. Known as "double-probing," this technique can compromise the signal environment, affecting the very measurements you are trying to make. For example, connecting two probes to the test point at once can create unacceptable levels of signal loading; connecting them one at a time exposes the test point to twice the risk of damage or misconnection. Moreover, it is time-consuming to connect two separate probes to the device under test.

Some logic analyzers have the ability to measure timing and state acquisitions through the same probe at the same time. This simultaneous timing/state acquisition speeds troubleshooting and supports signal integrity analysis work by minimizing the impact of probes on the system under test.

Recent advancements have taken probing technology to a new level. The latest generation of logic analyzer probes can carry digital (both timing and state) information to the logic analyzer, and also deliver these same signals to an oscilloscope as analog signals. One logic analyzer probe handles every aspect of the signal. Any pin of the probe can be used for both digital acquisition and analog acquisition. The analog signal routes through the logic analyzer to an external oscilloscope. By this means, it is possible to determine almost instantly whether a digital error is associated with an analog fault.

In high performance digital systems, a dedicated test point is usually the most practical way to measure signals. Some such test points are fitted with pins to simplify connection with clip-on probes and leadsets. These types of test connectors have an effect on the target device's signal environment, even when it is not connected to a logic analyzer.

A logic analyzer's probes can mount to dedicated connectors on the system under test. The compact Mictor connector, a high-density connector that is joined to a matching connector on the logic analyzer probe, is used in this application. Board-mounted connectors provide fast, positive connections but add cost to the target device and can affect high-speed signal operation.

High-density (HD) compression logic analyzer probes and D-Max™ probing technology have emerged to provide an alternative to conventional Mictor probe connectors. These new probes require no connectors on the device under test. Instead, they mate directly to land pads on the circuit board. **Figure 4** shows a D-Max™ connectorless probe installed on a circuit board. Held in place by threaded inserts, these probes address lead inductance as well as offer very low capacitive loading—only 0.5 pF. In addition, they provide both single-ended and differential measurements with no tradeoffs in channel count. These D-Max™ connectorless probes have the least effect on the signal of any logic analyzer probing scheme.
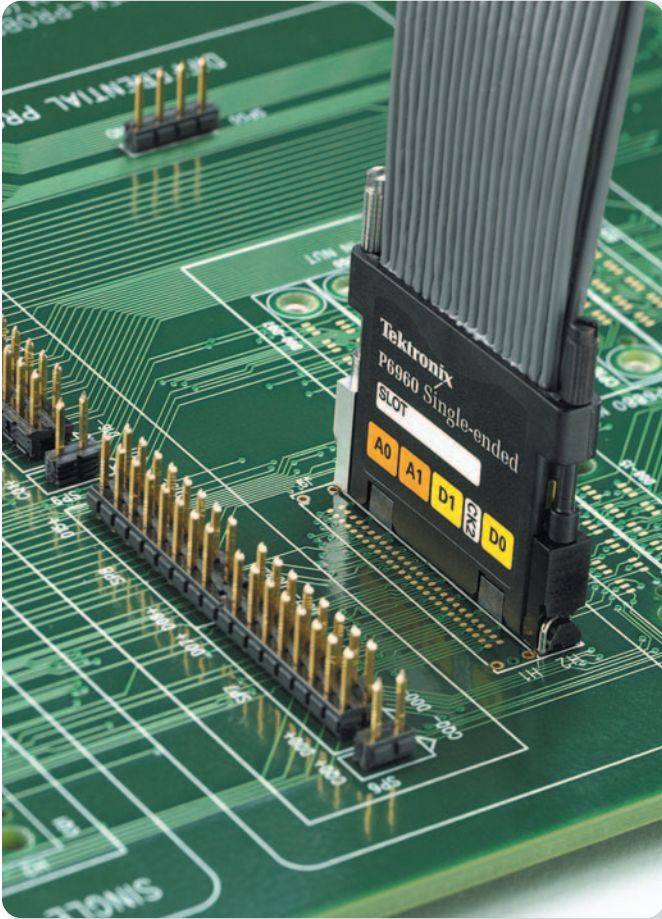
▶ **Figure 4.** *The new D-Max™ connectorless analyzer probe architecture provides a simple connection that delivers high fidelity signals from the system under test to the instruments.*

A D-Max™ connectorless logic analyzer probe has much less impact on the circuit board than does a Mictor-style connection, but land pads still must be designed into the board layout. The location at which a bus is probed can make a difference in the appearance of the signals. Therefore it is usually preferable to place test connection points close to the receiving devices, where the signals exhibit the characteristics that will be "seen" by the logic ICs. The D-Max™ connectorless probing technology's small footprint offers flexibility in this placement.

Digitizing Oscilloscopes Uncover Analog Aberrations

The other half of the signal integrity measurement analysis solution is the digitizing oscilloscope. This is the instrument you will use to track down the analog problems once they have been captured (in their digital form) by the logic analyzer. Digitizing oscilloscopes come in several forms, namely the digital storage oscilloscope (DSO), the digital phosphor oscilloscope (DPO), and the sampling oscilloscope.

Among the most valuable assets of a DSO or a DPO is its ability to acquire a one-time, "single-shot" event. The DSO or DPO captures the analog characteristics of the signals it is connected to. It can display a square wave, a transient spike, or a pure sine wave with equal ease and accuracy. It can trigger on the signal being viewed, on a synchronizing signal from the system under test, or upon receiving a command from an attached instrument such as a logic analyzer.

Another benefit is the movable probe. While the logic analyzer normally connects to the system under test via a fixed connector (or in the case of the latest generation of instruments, a fixed connector-less test point), the oscilloscope typically uses movable high-bandwidth probes, single-ended or differential probes, or even current probes.

It is common for many digitizing oscilloscopes to offer their maximum sample rate on one input, half that rate on two, and only $\frac{1}{4}$ the full sample rate when all four inputs are in use. Reducing the sample rate can impact the quality of the acquisition. At reduced sample rates, fewer samples of each measured waveform cycle are taken, making it more difficult to accurately reconstruct the acquired waveform. Even though the oscilloscope's input amplifier bandwidth remains unchanged, the quality of the acquisition suffers when lower sample rates are used. Obviously this is counterproductive when analyzing signal integrity with an oscilloscope!

Oscilloscope Feature	Recommended Capability for SI Analysis
Bandwidth/Rise Time	6 GHz bandwidth, 70 ps rise time, real time, single-shot
Sample rate	20 GS/s, full sample rate on multiple channels
Channels	4
Triggering	Low-jitter trigger with logic, setup/hold violation, and serial triggering
Record length	240,000 points (simultaneously on multiple channels)
Channel deskew	Ability to align the inputs of all channels expediently
Delta time accuracy	1.5 picoseconds RMS
Probing	6 GHz movable probe, or HD compression fixed probe through logic analyzer
Display	Color
Integration	Time-aligned high-speed oscilloscope traces with logic analyzer traces in one display
Automation and analysis	Automated measurement packages for jitter, bus standards, etc.

▶ **Table 3.** *Key digitizing oscilloscope specifications for signal integrity troubleshooting and analysis.*

Present-day DSOs address these sample rate effects by sampling at three to five times the bandwidth of the oscilloscope, and doing so on multiple channels simultaneously. This ensures adequate sampling points even when all channels are being used. Today, the best available single-shot sample rate performance for a digitizing oscilloscope is 20 GS/s on each channel.

Why is this so important? Imagine probing a test point with a conventional DSO that has a high sample rate, but lacks the ability to maintain that sample rate on multiple inputs. When you connect the first test point, the signal edge's rise time is clear and legible at 400 picoseconds (for example). When you enable the second input on a second test point's signal, *both* signals show a slower rise time and more aberrations. This is because the sample rate is cut in half, causing undersampling. This prevents the oscilloscope from accurately capturing a 400 picosecond edge rise time.

Undersampling causes the added aberrations and slower rise time. This inaccurate (and misleading!) waveform reconstruction is known as "aliasing." The best way to avoid aliasing is to use an instrument that delivers full single shot performance on all channels being used.

The oscilloscope, like the logic analyzer, must meet rigorous performance guidelines if it is to be used for signal integrity measurements. **Table 3** summarizes some key specifications.

The triggering functions in the DSO are every bit as critical as those in the logic analyzer. Like the logic analyzer, the oscilloscope's trigger is proof that a specified type of event occurred. The DSO triggering differs in its ability to detect and respond to a host of analog events:

▶ Edge levels and slew rate conditions

▶ Pulse characteristics including glitches, low-amplitude events, and even width conditions

▶ Setup and hold time violations

▶ High-speed serial digital patterns

All of these trigger types can assist engineers in first detecting, then tracking down signal integrity problems. There are also various combinations of voltage, timing, and logic triggers, as well as specialty triggers for applications such as USB 2.0 compliance testing.

Oscilloscope Probing Solutions

Even more than the logic analyzer probe, the oscilloscope probe is a critical element in signal integrity analysis measurements. The oscilloscope probe must, in effect, bring the system's full bandwidth and step response performance to the test point. At the same time, it must be durable, and compact enough to probe densely packed circuit boards. During troubleshooting for signal integrity problems, it is usually necessary to have one probe "fixed" on a test point at which an error appears (this may be the analog probe on the logic analyzer, if available), and one probe that can follow the signal path to track down the source of the problem.

Two important characteristics of a probe for high-speed work are the probe's capacitance and inductance. Every probe has resistance (R), inductance (L), and capacitance (C). The effect of capacitance and inductance, however, increase with frequency. Their combined effects can change the signal and the results of the measurement.

Figure 5 demonstrates the probe loading effects on a typical high-speed signal (ground-referenced 250 mV step with ~200 ps rise time). This screen shows the same signal—loaded and unloaded on a 4 GHz oscilloscope. The addition of the probe has loaded the original signal (white trace), as shown by the green trace, with the front corner of the step being slowed somewhat. Simply stated, as C and L increase, loading on the signal increases. Similarly, lead length inductance can cause serious distortion in the signal being measured.

Probe input characteristics and lead length inductance can actually *cause* signal integrity problems. One might, for example, conclude that the bus itself is degrading the rise time of the digital signal and causing logic errors. By switching to a lower-capacitance probe, it becomes clear that the rise time is not degraded after all. The logic error has a different cause: probing effects! **Figure 5** shows how probing effects can slow down an edge, even to the point of causing errors that did not exist before.
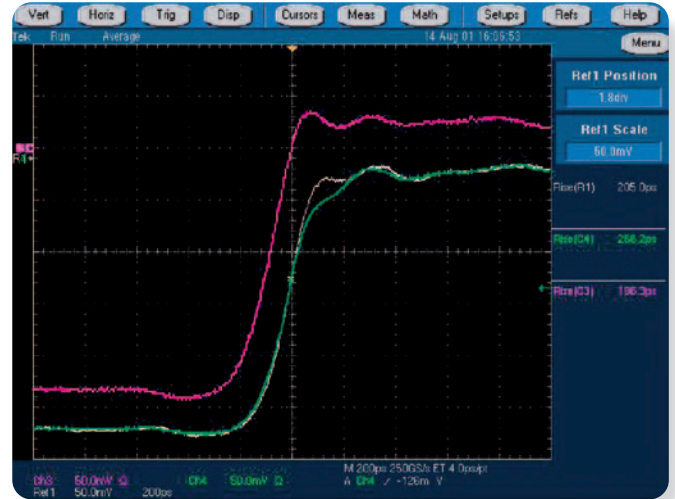
▶ **Figure 5.** *The probe loading effects on a high-speed signal.*

A new generation of ultra-low-capacitance oscilloscope probes is the answer to signal integrity and high-speed measurement problems. With 6 GHz bandwidth at the probe tip, very short probe tip lead lengths, and less than 0.5 pF input capacitance, these new probes better preserve the signal as it travels to the oscilloscope input. They bring the signal, aberrations and all, accurately to the acquisition system.

The probe's performance is critical because it is the first link in a chain of measurement subsystems that must preserve, capture, and display the signal as accurately as possible. A low-capacitance probe with very short probe tip and ground lead lengths ensures that the bandwidth of the oscilloscope is not wasted.

The Importance of Oscilloscope Bandwidth

Oscilloscope bandwidth is an indispensable ingredient in any signal integrity troubleshooting process. This short tutorial will explain why it is essential to use an instrument with the highest bandwidth available.

We have already discussed the signal characteristics that define high-speed signal integrity problems. Many of them show up during signal transitions, or as unwanted transients that result from timing violations. It is critical to capture these edges and transients as accurately as possible. And that takes bandwidth.

Oscilloscope bandwidth is traditionally specified at the –3 dB frequency response point for a sine wave. **Figure 6** tells the story. Here, a 1 GHz oscilloscope has an increasing amplitude error as the sine wave frequency climbs toward the 1 GHz mark. At its bandwidth-rated sine wave frequency, the amplitude error is –3 dB, or almost 30%.
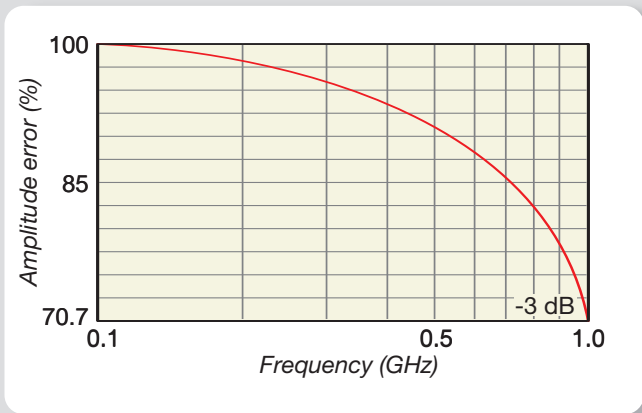
► **Figure 6.** *Frequency response plot for a typical 1 GHz oscilloscope.*

An oscilloscope with insufficient bandwidth for the measurement task will take a toll on digital signal rise and fall time measurements. Given the dramatically decreasing transition times in today's digital technologies, this is a critical factor in choosing appropriate measurement tools.

To understand this concept, consider this "one-pole model" for oscilloscope input rise time with a high-speed step signal:

$$\text{Oscilloscope Rise Time} \quad \frac{0.35^{*1}}{\text{Oscilloscope Bandwidth}}$$

For a modern oscilloscope, where bandwidth x rise time ~0.42, this equates to about 210 picoseconds for a 2 GHz oscilloscope and about 84 ps for a 5 GHz instrument. A general formula for the net measured rise time produces the step response characteristic:

$$\text{Measured Rise Time} = \sqrt{(\text{Oscilloscope Rise Time})^2 + (\text{Signal Rise Time})^2}$$

Using these formulas, it can be shown in Figure 7a and 7b that a signal having 85 picoseconds actual rise time will present a rise time of about 135 ps when measured with a 4 GHz bandwidth oscilloscope (using BW x RT = 0.42). A 6 GHz oscilloscope reduces the measured rise time to about 110 ps, dramatically improving the accuracy of the reading.

*1 *The constant in this formula can range from 0.35 for a one-pole model to 0.45 for a brick wall filter. Typical value for a modern high bandwidth oscilloscope is 0.42.*
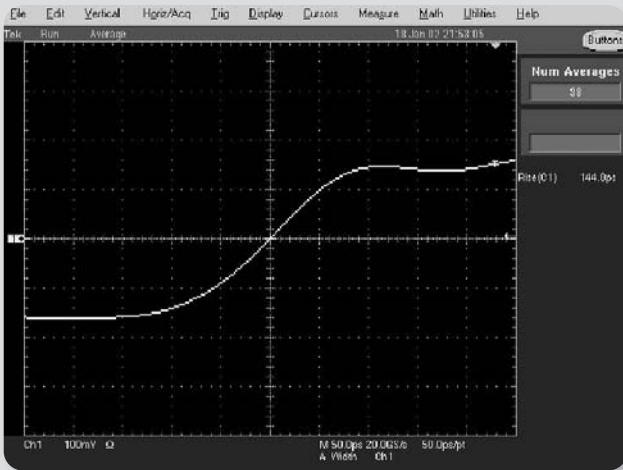
▶ **Figure 7a.** *Measurement results for a pulse edge with 85 ps actual rise time on a 4 GHz TDS7404 DPO.*
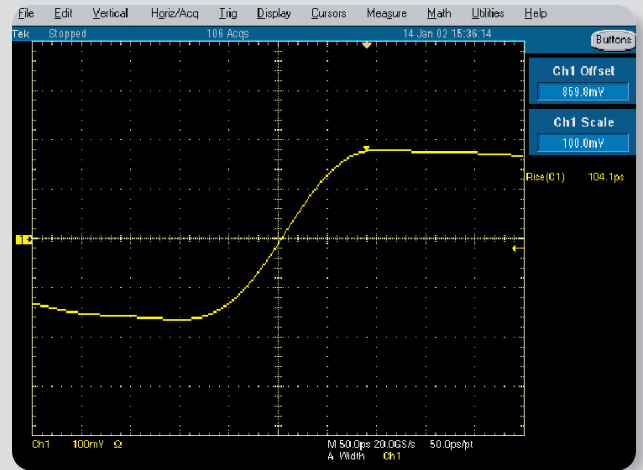
▶ **Figure 7b.** *Measurement results for a pulse edge with 85 ps actual rise time on a 6 GHz TDS6604 DSO.*

Summarizing the bandwidth and step response discussions, in both cases the calculated figures and real-world measurements confirm that oscilloscope bandwidth makes a difference in the results you see on the screen. With so many system-level problems being the direct result of edge effects and aberrations, an oscilloscope whose bandwidth is 3 to 5 times that of the measured signal is the right tool for signal integrity troubleshooting.

Integrated Logic Analyzers and Oscilloscopes Identify Signal Integrity Problems

The logic analyzer and the DSO are two powerful tools in the signal integrity troubleshooter's kit. But with recent advancements in integration, the power of the two individual tools has been multiplied.

New integrated viewing tools make it possible to connect a DSO (that meets the analog bandwidth needs of your target device) to a logic analyzer (with adequate channel count, memory depth, and sample rate) to handle the analog and digital measurement requirements. Once connected, the two instruments work together seamlessly. The logic analyzer display screen presents digital information as well as the oscilloscope's analog waveform.

The two waveforms are time-aligned so that the digital waveform can be examined with its analog waveform. For example, in the **Figure 8** display the time-correlated digital and analog waveform measurements provide four different views of the same signals. The top two waveforms are 4-bit and 8-bit bus waveforms with red flags indicating the locations of several glitches. The next two waveforms are individual signal lines that are part of the top two bus waveforms. The red flags on these two signals indicate glitch locations. The next two waveforms are high-resolution timing waveforms showing the details that the glitches are related to the leading edges of the other signal. The last two waveforms are the analog waveforms from the oscilloscope of the same two signal lines All of these waveforms are time-correlated and are on the same display. It is quickly seen that the two signal lines have crosstalk by analyzing the time-correlated views of the digital and analog waveforms.
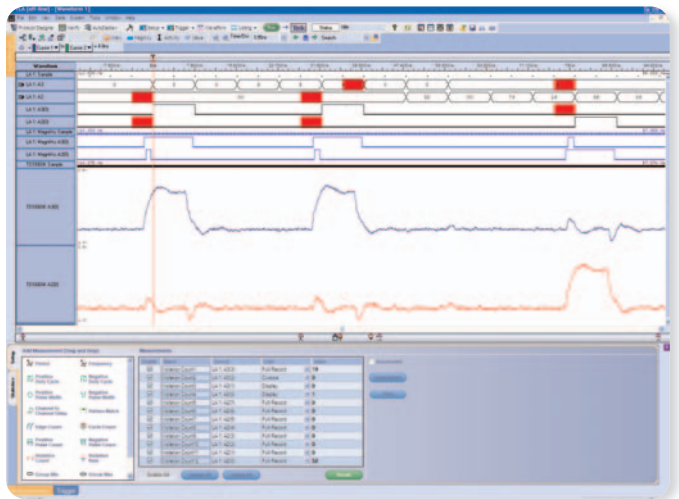
▶ Figure 8. *Crosstalk errors quickly identified with time-correlated digital and analog measurements on the same display.*

Integrated viewing is a valuable capability, but remember that the analog information on the screen is only as accurate as the bandwidth and step response performance of the oscilloscope being used. That is why it is important to select tools that allow you to match the digitizing oscilloscope capabilities to the needed digital measurement performance level.

Jitter Analysis Tools Simplify Complex Measurements

Signal integrity analysis is not always a matter of finding a slow edge or low signal amplitude somewhere in the system. As explained earlier, factors like jitter can play a large role in system stability. Jitter typically originates in the clock circuitry but can also arise from power supply noise, crosstalk, and Phase Lock Loop (PLL) circuits. Jitter can affect data, addresses, enable lines, and more—in fact, virtually any signal in the system.

Jitter measurements have become increasingly challenging with new high-speed digital designs. Today's jitter measurement requirements include cycle-to-cycle measurements (rather than cumulatively over many acquisitions), timing trend analysis, statistics with histograms, measurements on spread-spectrum clocks, serial data stream analysis, and more. High-speed signals, with their fast rise times and small timing budgets, call for jitter measurement accuracy in the 1 ps RMS range.

Clearly this level of performance requires a fast, stable oscilloscope. No less important is the software tool set that supports jitter measurements. Because jitter comes in so many forms, and because jitter measurements rely heavily on statistical calculations, a dedicated software jitter package is a good solution for efficient signal integrity work. The latest packages integrate into high-bandwidth digitizing oscilloscopes and can make timing measurements on every cycle within a single acquisition. These timing analysis packages can also accumulate statistical analysis data over multiple acquisitions. **Figure 9** illustrates a typical jitter measurement screen. The menu bar and soft buttons guide you through the measurement steps, while statistical results are clearly displayed in tabular form in the lower half of the window.
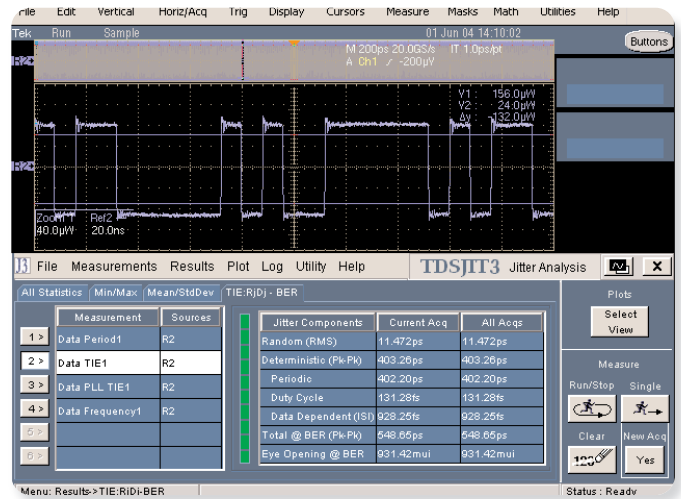
▶ **Figure 9.** *Jitter measurement application screen.*

The timing measurement analysis software must of course be coupled with an oscilloscope that itself adds as little jitter as possible to the signal. Trigger jitter on the order of 7 ps RMS is desirable for most data transmission standards. Other important characteristics include Delta Time accuracy in the range of 1.5 ps RMS, and of course high bandwidth with oversampling. An oscilloscope with 6 GHz bandwidth and 20 GS/s single-shot sample rate on multiple channels meets the key high-speed specification requirements for high-speed jitter measurements on fast digital buses and devices.

Signal Integrity Troubleshooting

In this primer, we have examined the cause and effect of signal integrity-related problems in digital systems. In the course of our discussion, we have looked at how to get the best signal fidelity from your test and measurement equipment to solve these problems.

Now we will use three design situations to illustrate the tools and techniques needed to resolve elusive real-world signal integrity challenges in the design environment.

Application Examples
Situation I

A quality problem has shown up on a digital system board that is just entering the manufacturing phase. The board is at the heart of the company's new flagship product, a sophisticated machine controller, and must be announced on schedule since it has received considerable advance publicity in its market.

Early production samples are experiencing intermittent failures. The failures are appearing on the board's system bus, but they do not seem to originate there. The system bus is bi-directional, with multiple devices sending and receiving data across it. Because the board is central to the whole system's operation, manufacturing cannot proceed until the problem is solved.

The system operates at "medium" speeds. But because much of the logic has fast rising and falling edges, signal integrity problems must be considered. Other possibilities range from logic errors to layout problems.

The design team, knowing that built-in debug features can save precious troubleshooting time, campaigned to get logic analyzer test points built into the board. It was a controversial proposal, since the dense, compact board design lacked space for conventional connectors. Because the design team was using a Tektronix TLA7AA3 logic analyzer for troubleshooting, they were able to fit the land pattern within the allowable space.

Setup

▶ TLA7012 logic analyzer mainframe

▶ TLA7AA3 102-channel logic analyzer acquisition module

▶ P6860 HD single-ended logic analyzer probe

▶ TDS6604 DSO

▶ iView™ interface

The troubleshooting setup takes advantage of the TLA7AA3 logic analyzer's ability to route analog signals through the logic analyzer probe, acquire them with the oscilloscope, and display those signals on the logic analyzer screen.

The logic analyzer is set to trigger on the READ instruction that produces a faulty data value.

Discovery

The logic analyzer screen displays the timing waveforms of selected signals on the bus and reveals the problem in the signal that is causing the error. The instrument's high-resolution (8 GHz, 125 ps) timing waveform makes it clear that there is not a timing problem with the data being read (the 031:DATA trace). However, that address seems erratic, with occasional "skipped" locations that imply a problem in the least significant bit—Address 0. This leads the engineer to select an analog view of the AD0 bus line.

The time-aligned analog trace at the bottom of the screen reveals the true signal integrity problem. The TDS6604 oscilloscope acquires the signal through the logic analyzer's P6860 HD single-ended probe, then displays it on the logic analyzer with the iView™ interface.
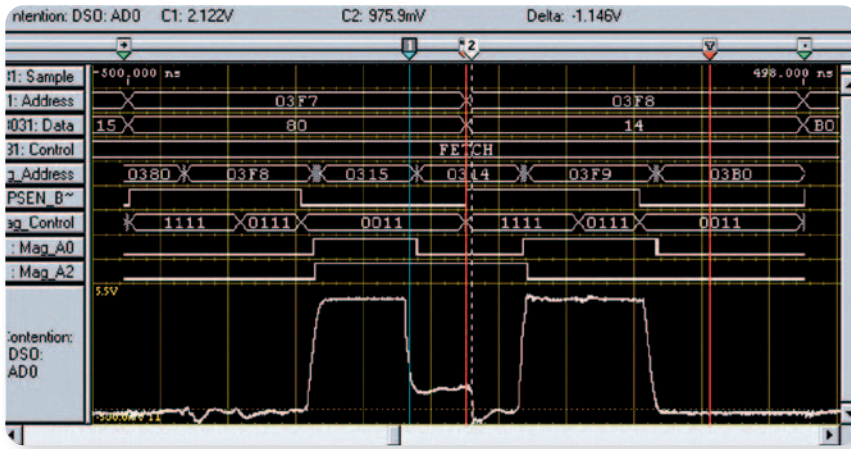
▶ **Figure 10.** *The analog trace reveals an invalid logic level (software cursor 1 and 2) that is causing digital problems in the system.*

In this case, the AD0 (Address 0) signal's logic level is invalid at the time it is clocked. It is neither high nor low. Suspecting a bus contention problem, the engineer follows the bus until he discovers that due to a design error, two devices on the address line are enabled at the same time.

This procedure demonstrates how digital timing problems are sometimes best traced by looking at the signals in the analog domain. It also provides a lesson about planning for test points. Without proper logic analyzer connection points, it might have been difficult to acquire the signal with enough signal fidelity to assess the bus contention.

Situation II

The new motherboard for a next-generation server is suffering from unexplained, intermittent problems. Its first and second prototypes run reliably at low clock rates. When brought up to the specified clock rate, seemingly random failures appear.

Board layout-related problems are suspected but have been difficult to prove with conventional tools. The project schedule calls for just two rounds of prototype boards, but unless the intermittent problem can be found, a third prototype may be required. This added time and cost puts the success of the new product at risk.

Like most complex digital designs, the board includes logic analyzer test points. These points are fitted with Mictor connectors that are compatible with the TLA700 Series logic analyzer probing.

Setup

▶ TLA7012 logic analyzer mainframe

▶ TLA7AA4 136-channel logic analyzer acquisition module

▶ P6860 HD single-ended logic analyzer probe

▶ P6860 HD compression-to-Mictor adapter

▶ iView™ interface

▶ TDS7104 digital phosphor oscilloscope

Discovery

Intermittent problems are often caused by signals that "are not supposed to be there," called glitches. Suspecting this, the engineer sets the TLA7AA4 to trigger on glitches, one of its many triggering functions.

The TLA7AA4 logic analyzer detects a glitch during the Pre-fetch cycle on a signal line named IFETCH. The logic analyzer triggers and flags the point in time at which the glitch occurs. The Mag_IFETCH trace clearly displays a narrow pulse.
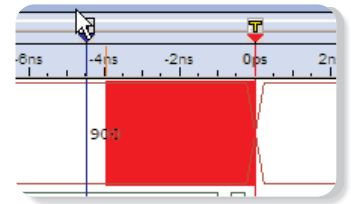
▶ Glitch detected and flagged on signal.

▶ 125 ps MagniVu™ trace showing glitch in greater detail.

▶ Up to 20 GS/s analog trace captured on TDS and transferred to TLA display showing cause of glitch.

▶ Overlay multiple waveforms for complete visual comparisons.
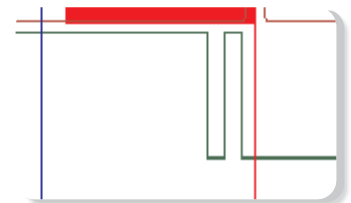
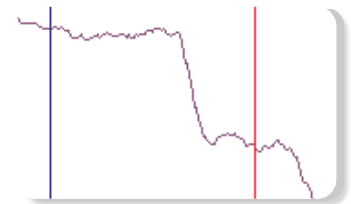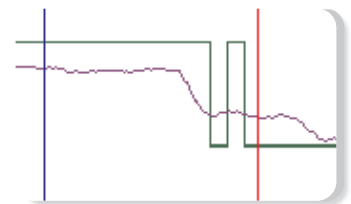▶ Digital Waveform

▶ Analog Waveform

▶ Overlay of Digital and Analog Waveforms

▶ **Figure 11.** *The iView™ screen shows a glitch on the first waveform trace (second from top) that results from a momentary threshold crossing on the IFETCH line (third from top) due to termination reflections.*

The 125 ps resolution of the MagniVu™ high resolution timing acquisition ensures accurate capture of the pulse time and duration.

The glitch trigger also causes an acquisition on the TDS7104 oscilloscope which is integrated with the logic analyzer via the iView™ interface. The oscilloscope uses the logic analyzer's iConnect™ probing to measure the same signal.

The resulting analog acquisition appears at the center of the logic analyzer screen showing the true nature of the glitch. This glitch is an analog aberration that briefly crosses above and then below the logic threshold, creating a valid high logic level that lasts just long enough to create the glitch problem.

Armed with this understanding of the analog problem, the engineer determines that the board layout in the area of this signal line is prone to termination reflections as edge speed increases. A re-layout corrects the problem.

Situation III

A fast new workstation prototype has a Phase Lock Loop (PLL) oscillator configured as a "zero delay" clock source for its memory system. The PLL receives an external clock signal, locks on to the frequency, and retransmits the signal through a clock distribution network to the memory elements. In doing so, it corrects for all the known delays along the distribution path.

However, the memory seems to store incorrect data occasionally. This is believed to be due to a timing error in the clock, which is causing data to get clocked into the memory at the wrong time—before all the data lines are "ready." What is the nature of the timing error? What is its origin? The solution to a system-wide problem depends on the answer to these questions.

Setup

▶ TLA5204 logic analyzer

▶ P6418 logic analyzer probe

▶ TDS6604 DSO

▶ P7260 high-bandwidth movable probe for TDS6604

▶ TDSJIT3 Jitter and Timing Analysis Software

Discovery

After observing the digital errors with the TLA5204 logic analyzer, the engineer suspects an instability in the clock signal coming from the PLL oscillator. Though intermittent, the error does not appear to be completely random.

A real-time jitter measurement is found to be the most productive solution. Connecting a P7260 probe to the clock signal, the engineer takes several measurements at a 20 GS/s sample rate and concatenates them in the on-board TDSJIT3 application. Comparing the sample on a cycle-to-cycle
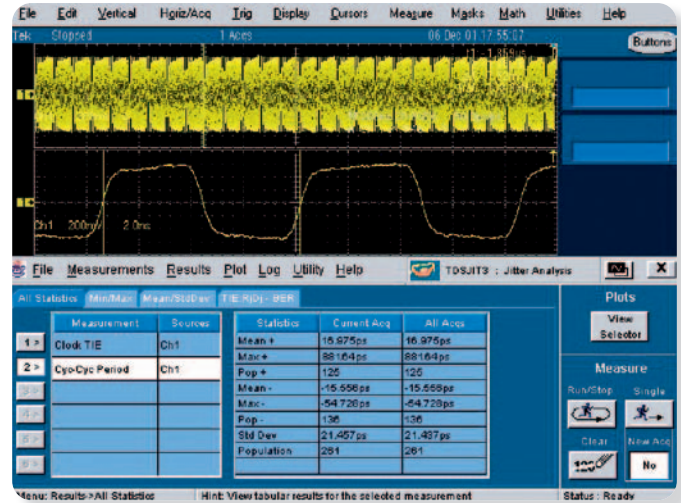
▶ **Figure 12.** *This TDSJIT3 measurement screen includes several concatenated jitter measurements taken at 20 GS/s. It reveals a PLL signal that has almost 1 ns of error within a 7.5 ns cycle.*

basis using the Cyc-Cyc Period measurement and the Cycle Trend function in TDSJIT3, it becomes clear that the PLL is staying within its frequency tolerance most of the time, but jumping ahead occasionally as though correcting a frequency drift. In **Figure 12,** the error amounts to almost 1 ns within a 7.5 ns cycle.

A second TDSJIT3 function helps pinpoint the source of the PLL's behavior. Using the application's FFT tools, it is found that there is an unexpected energy peak at 120 kHz. A quick look at the system schematic reveals that this is the frequency of the system's switched power supply. From there, it is a simple matter to filter the offending frequency out of the PLL's supply connection.

Summary

Signal integrity measurements have become a critical step in the process of developing digital systems. In today's fast systems, a tiny timing error on the controller data bus can ripple all the way through the system and show up as a fault on a serial I/O bus. The design engineer is responsible for tracking down and eliminating these problems anywhere in the system.

To do so, he or she will need a powerful measurement tool set that has the bandwidth and time-saving features to properly address high-speed signal aberrations. These tools include digitizing oscilloscopes, logic analyzers, high-fidelity probes, and analysis software.

Innovative measurement solutions such as HD compression probes, application-specific jitter software, and integrated logic analyzer/oscilloscope waveform viewing have emerged to help the designer trace signal integrity-related problems. With these powerful tools in hand, the engineer can locate faults and follow them to their source quickly.

Until recently, unseen signal integrity problems were frequently to blame for schedule delays and reliability issues in new digital products. Now the designer has the means to defeat even the toughest signal integrity challenges.

Fundamentals of Signal Integrity

▶ Primer

Our most up-to-date product information is available at:
www.tektronix.com

Product(s) are manufactured
in ISO registered facilities.

9/05   FLG/PG   55W-15465-4

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